LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A signal conversion system, comprising:

a memory system programmed to provide a set of digital output samples in response to a given digital input sample, each of a plurality of possible input samples being associated with a corresponding set of plural digital output samples; and

an aggregator that aggregates the output samples and provides an aggregated output stream signal at a desired output sample rate, which is different from an input sample rate.

2. (Original) The conversion system of claim 1, the memory system being programmed to provide N output samples that represent delta-sigma modulated data in response to the given digital input sample, where N is a positive integer greater than one.

3. (Original) The conversion system of claim 1, the memory system operating at a rate that is less than the desired output sample rate.

4. (Original) The conversion system of claim 1, the memory system further comprising a look-up table programmed to store output data indexed by address data defined as a function of the possible input samples, the address data being functionally related to at least one of state information and outputs of delta-sigma modulation represented by the look-up table, the look-up table providing the set of output samples as a vector of outputs in response to the given input sample, whereby the look-up table can operate in real-time at rates that are slower than would be required for the delta-sigma modulation being represented by the look-up table.

5. (Original) The conversion system of claim 4, the memory system further comprising a buffer that receives a digital input signal and buffers a selected portion of the input signal as the given input sample to define the address data for the look-up table.

6. (Original) The conversion system of claim 1, at least a portion of data stored in the memory system being compressed data.

7. (Original) The conversion system of claim 6, at least a portion of the compressed data having been compressed by delta-sigma modulation.

8. (Original) The system of claim 1, further comprising a delta-sigma modulator operative to receive at least one digital input signal and provide corresponding quantized output data that defines the plurality of input samples provided to the memory system at an input sample rate that is less than the output sample rate.

9. (Original) The system of claim 8, the quantized output data being generated based on S input samples, where S >=1, to address the memory, such that the memory runs at 1/S times slower than the delta sigma modulator.

10. (Original) The system of claim 8, the delta-sigma modulator further comprises a complementary metal-oxide semiconductor (CMOS) delta-sigma modulator.

11. (Original) The system of claim 1, further comprising a digital-to-analog converter that converts the aggregated output stream signal to a corresponding analog signal having a center frequency functionally related to the desired output sample rate.

12. (Original) A transmitter in combination with the system of claim 11, the combination comprising an antenna operative to propagate a wireless signal at a transmission frequency based on the corresponding analog signal.

13. (Original) The system of claim 11, the digital-to-analog converter provides the analog output signal tuned directly at a center frequency that defines a desired radio transmission frequency.

14. (Original) The system of claim 1, further comprising:

a separator operative to split the input samples into in-phase and quadrature components thereof;

memory system further comprising:

a first memory system that stores look-up table data representing delta-sigma modulated outputs indexed to provide in-phase components of the output samples based on in-phase components of the input samples; and

a second memory system that stores look-up table data representing delta-sigma modulated outputs indexed to provide quadrature components of the output samples based on quadrature components of the input samples; and

an aggregator that aggregates the in-phase and quadrature components of the output samples to provide the aggregated output stream at the desired output sample rate.

15. (Previously Amended) A conversion system, comprising:

a buffer that buffers a portion of a digital input signal as a digital input sample at an input sample rate;

a look-up table programmed to provide a set of digital output samples in response to at least one digital input sample, the at least one digital input sample defining address data for the look-up table, the look-up table providing the set of digital output samples at a sample rate which is different from that of the at least one digital input sample;

an aggregator that aggregates the output samples and provides an aggregated output stream of digital data; and

a digital-to-analog converter that converts the aggregated output stream to a corresponding analog signal at a desired output sample rate.

16. (Original) The system of claim 15, further comprising a delta-sigma modulator operative to receive a second digital input signal and provide corresponding quantized output data at the input sample rate to define the digital input signal.

17. (Original) The system of claim 16, the delta-sigma modulator further comprises a complementary metal-oxide semiconductor (CMOS) delta-sigma modulator.

18. (Currently Amended) A transmitter in combination with the system of ~~claim 14~~ claim 15, the combination comprising an antenna operative to propagate a wireless signal at a transmission frequency based on the corresponding analog signal.

19. (Currently Amended) The system of ~~claim 14~~ claim 15, further comprising:

a separator operative to split the input signal into in-phase and quadrature component samples thereof;

the buffer comprising a pair of buffers, each being operative to buffer a respective one of the in-phase and quadrature component samples in parallel with each other;

the look-up table comprising a pair of look-up table, each being operative to provide plural digital output samples in response to receiving a respective one of the buffered in-phase and quadrature component samples; and

the aggregator being operative to aggregate the in-phase and quadrature components of the output samples from the pair of look-up tables to provide the aggregated output stream of digital data.

20. (Original) The system of claim 15, at least a portion of the data stored in the memory system being compressed data.

21. (Original) The system of claim 20, at least a portion of the data stored in the memory system having been compressed by delta-sigma modulation.

22. (Cancelled)

23. (Original) A conversion system, comprising:

means for storing look-up table data representing delta-sigma modulated outputs indexed according to corresponding input samples each having a predetermined number of bits; and

means for aggregating output samples provided by the means for storing and for providing an aggregated output data stream at a desired output sample rate.

24. (Original) The system of claim 23, further comprising

means for splitting an input signal into in-phase and quadrature components;

the means for storing further comprising:

first means for storing look-up table data representing delta-sigma modulated outputs and for providing output samples based on the in-phase components of the input signal; and

second means for storing look-up table data representing delta-sigma modulated outputs and for providing output samples based on the quadrature components of the input signal;

the means for aggregating being operative to aggregate the output samples from the first and second means to provide the aggregated output stream at the desired output sample rate.

25. (Original) The system of claim 24, further comprising means for converting the aggregated output stream to an analog signal that is centered at about a desired radio transmission frequency.

26. (Original) The system of claim 25, the means for converting further comprising a one-bit digital-to-analog converter.

27. (Original) A method for generating a memory construct that can emulate a delta-sigma modulator, comprising:

performing delta-sigma modulation on each of a plurality of input samples to provide corresponding output samples for each of the plurality of input samples; and

storing look-up table data that includes at least a substantial portion of the output samples and the plurality of input samples; and

programming a memory device based on the stored look-up table data so that the memory device is operative to emulate the delta-sigma modulation by providing a corresponding vector of the output samples in response to each of the input samples.

28. (Original) The method of claim 27, the further comprising compressing at least a portion of the stored look-up table data.

29. (Original) The method of claim 27, the compression further comprising performing delta-sigma modulation on the stored look-up table data.